Modulation and Control of Transformerless UPFC

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***Abstract*—In this paper, a modulation and control method for the new transformerless unified power flow controller (UPFC) is presented. As is well known, the conventional UPFC that consists of two back-to-back inverters requires bulky and often complicated zigzag transformers for isolation and reaching high power rating with desired voltage waveforms. To overcome this problem, a completely transformerless UPFC based on an innovative configuration of two cascade multilevel inverters has been proposed. The new UPFC offers several advantages over the traditional technology, such as transformerless, light weight, high efficiency, low cost and fast dynamic response. This paper focuses on the modulation and control for this new transformerless UPFC, including optimized fundamental frequency modulation for low total harmonic distortion and high efficiency, independent active and reactive power control over the transmission line, dc-link voltage balance control, etc. The new UPFC with proposed control method is verified by experiments based on 4160-V test setup. Both the steady-state and dynamic-response results will be shown in this paper.**

***Index Terms*—Flexible ac transmission systems (FACTS), multilevel inverter, power flow control, transformerless, unified power flow controller (UPFC).**

I. Introduction

THE unified power flow controller (UPFC) is able to control, simultaneously or selectively, all the parameters affecting power flow in the transmission line (i.e., voltage magnitude, impedance, and phase angle) [1]–[3]. The conventional UPFC consists of two back-to-back connected voltage source inverters that share a common dc link, as shown in Fig. 1. The injected series voltage from inverter-2 can be at any angle with respect to the line current, which provides complete flexibility and controllability to control both active and reactive power flows over the transmission line. The resultant real power at the terminals of inverter-2 is provided or absorbed by inverter-1 through the common dc link. As a result, UPFC is the most versatile and powerful flexible ac transmission systems device. It can effectively reduce congestions and increase the capacity of existing transmission lines. This allows the overall system to operate at its theoretical maximum capacity. The basic control methods, transient analysis, and practical operation considerations for UPFC have been investigated in [4]–[10].

The conventional UPFC has been put into several practical applications [11]–[13], which has the following features: 1) both inverters share the same dc link; 2) both inverters need to exchange real power with each other and the transmission line; 3) a transformer must be used as an interface between the transmission line and each inverter. In addition, any utility-scale UPFC requires two high-voltage, high-power (from several MVA to hundreds of MVA) inverters. This high-voltage, high-power inverters have to use bulky and complicated zigzag transformers to reach their required VA ratings and desired voltage waveforms. The zigzag transformers are: 1) very expensive (30–40% of total system cost); 2) lossy (50% of the total power losses); 3) bulky (40% of system real estate area and 90% of the system weight); and 4) prone to failure [14]. Moreover, the zigzag transformer-based UPFCs are still too slow in dynamic response due to large time constant of magnetizing inductance over resistance and pose control challenges because of transformer saturation, magnetizing current, and voltage surge [15].

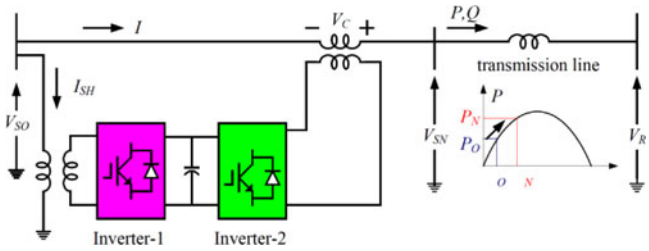

Fig. 1. Conventional UPFC.

Recently, there are two new UPFC structures under investigation: 1) the matrix converter-based UPFC [16]–[18] and 2) distributed power-flow controller (DPFC) derived from the conventional UPFC [19]. The first one uses the matrix converter replacing the back-to-back inverter to eliminate the dc capacitor with ac capacitor on one side of the matrix converter. The DPFC employs many distributed series inverters coupled to the transmission line through single-turn transformers, and the common dc link between the shunt and series inverters is eliminated. The single-turn transformers lose one design freedom, thus making them even bulkier than a conventional transformer given a same VA rating. In summary, both UPFCs still have to use the transformers, which inevitably cause the same aforementioned problems associated with transformers (such as bulky, lossy, high cost, and slow in response).

The cascade multilevel inverter (CMI) is the only practical inverter technology to reach high-voltage levels without the use of transformers, a large number of semiconductor devices (diodes), or a large number of capacitors [14], [20]–[22]. The CMI-based STATCOMs (up to $\pm$200 Mvar) have been installed in Europe and Asia [23]–[26]. However, the CMI could not be directly used in the conventional UPFC, because the conventional UPFC requires two inverters connected back-to-back to deal with active

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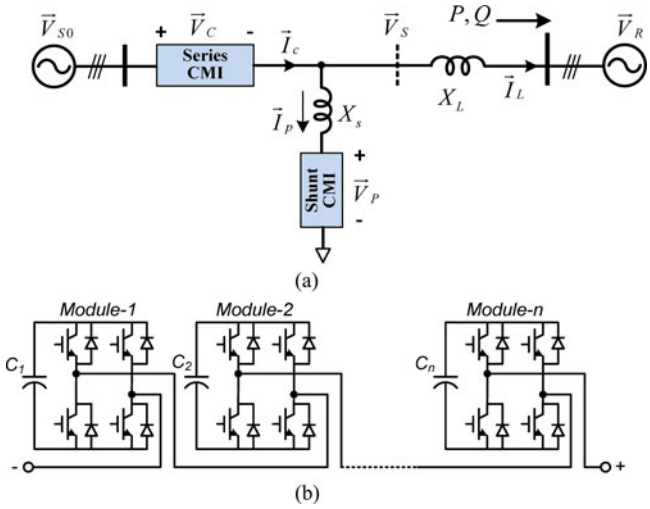

Fig. 2. New transformerless UFPC. (a) System configuration of transformerless UPFC. (b) One phase of the cascaded multilevel inverter.

TABLE I
MAIN SYSTEM PARAMETERS FOR 13.8-KV PROTOTYPE

Parameters	Value
System power rating	2 MVA
V_{s0} rms	13.8 kV
Max series CMI current, I_C rms	84 A
Max shunt CMI current, I_P rms	42 A
V_{dc} (Shunt)	600 V
V_{dc} (Series)	600 V
H-bridge dc capacitance	2350 μF
No. of H-bridges per phase (Shunt)	20
No. of H-bridges per phase (Series)	10

power exchange. To address this problem, a UPFC with two face-to-face connected CMIs was developed in [27] to eliminate the zigzag transformers that are needed in the conventional multipulse inverter-based UPFC. However, it still required an isolation transformer.

To eliminate the transformer completely, a new transformerless UPFC based on an innovative configuration of two CMIs has been proposed in [28]. The system configuration is shown in Fig. 2(a) and main system parameters for a 13.8-kV/2-MVA prototype (target system) is shown in Table I. As shown in Fig. 2(a), the transformerless UPFC consists of two CMIs, one is series CMI, which is directly connected in series with the transmission line; while the other is shunt CMI, which is connected in parallel to the sending end after series CMI. Each CMI is composed of a series of cascaded H-bridge modules as shown in Fig. 2(b). The transformerless UPFC has significant advantages over the traditional UPFC such as highly modular structure, light weight, high efficiency, high reliability, low cost, and a fast dynamic response. The basic operation principle, operation range, and required VA rating for series and shunt CMIs have been studied in [28]. Nevertheless, there are still challenges for the modulation and control of this new UPFC: 1) UPFC power flow control, such as voltage regulation, line impedance compensation, phase shifting or simultaneous control of

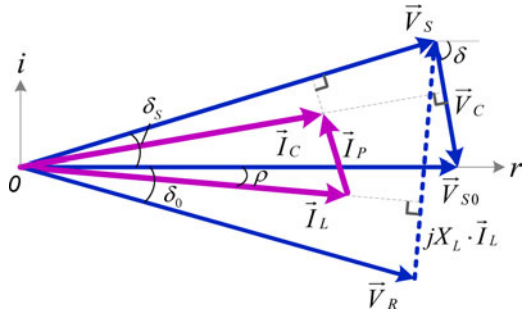

Fig. 3. Phasor diagram of the transformerless UPFC.

voltage, impedance, and phase angle, thus achieving independently control both the active and reactive power flow in the line; 2) dc capacitor voltage balance control for H-bridges of both series and shunt CMIs; 3) modulation of the CMI for low total harmonic distortion (THD) of output voltage and low switching loss; 4) fast system dynamic response. This paper presents the modulation and control for the new transformerless UPFC to address aforementioned challenges. The UPFC functionality with proposed control method is verified at low voltage level (4160 V), and both the steady-state and dynamic responses results will be shown in this paper.

II. OPERATION PRINCIPLE OF THE TRANSFORMERLESS UPFC

With the unique configuration of the series and shunt CMIs, the transformerless UPFC has some new features:

1) Unlike the conventional back-to-back dc link coupling, the transformerless UPFC requires no transformer, thus it can achieve low cost, light weight, small size, high efficiency, high reliability, and fast dynamic response.
2) The shunt inverter is connected after the series inverter, which is distinctively different from the traditional UPFC. Each CMI has its own dc capacitor to support dc voltage.
3) There is no active power exchange between the two CMIs and all dc capacitors are floating.
4) The new UPFC uses modular CMIs and their inherent redundancy provides greater flexibility and higher reliability.

Due to the unique system configuration, the basic operation principle of the transformerless UPFC is quite different from conventional UPFC. Fig. 3 shows the phasor diagram of the transformerless UPFC, where $\overrightarrow{V}_{S0}$ and $\overrightarrow{V}_R$ are the original sending-end and receiving-end voltage, respectively. Here, $\overrightarrow{V}_{S0}$ is aligned with real axis, which means phase angle of $\overrightarrow{V}_{S0}$ is zero. The series CMI is controlled to generate a desired voltage $\overrightarrow{V}_C$ for obtaining the new sending-end voltage $\overrightarrow{V}_S$, which in turn, controls active and reactive power flows over the transmission line. Meanwhile, the shunt CMI injects a current $\vec{I}_P$ to the new sending-end bus to make zero active power into both CMIs, i.e., to make the series CMI current $\vec{I}_C$ and the shunt CMI current $\vec{I}_P$ be perpendicular to their voltages $\overrightarrow{V}_C$ and $\overrightarrow{V}_S$, respectively. As a result, both series and shunt CMIs only need to provide the reactive power. In such a way, it is possible to apply the CMIs to the transformerless UPFC with floating dc capacitors for H-bridge modules.

The detailed operating principle of the transformerless UPFC can be formulated as follows. With referring to Figs. 2 and 3, the transmitted active power P and reactive power Q over the line with the transformer-less UPFC can be expressed as

$$\begin{aligned} P+jQ &= \overrightarrow{V}_R \cdot \left(\frac{\overrightarrow{V}_{S0}-\overrightarrow{V}_C-\overrightarrow{V}_R}{jX_L}\right)^* \\ &= \left(-\frac{V_{S0}V_R}{X_L}\sin\delta_0+\frac{V_CV_R}{X_L}\sin(\delta_0-\delta)\right) \\ &\quad + j\left(\frac{V_{S0}V_R\cos\delta_0-V_R^2}{X_L}-\frac{V_CV_R}{X_L}\cos(\delta_0-\delta)\right) \end{aligned} \quad (1)$$

where symbol * represents the conjugate of a complex number; δ_0 is the phase angle of the receiving-end voltage $\overrightarrow{V}_R$; $\delta$is the phase angle of the series CMI injected voltage $\overrightarrow{V}_C$; X_L is the equivalent transmission line impedance. The original active and reactive powers, P_0 and Q_0 with the uncompensated system (without the UPFC, or $V_C = 0$) are

$$\begin{cases} P_0 = -\frac{V_{S0}V_R}{X_L}\sin\delta_0 \\ Q_0 = \frac{V_{S0}V_R\cos\delta_0-V_R^2}{X_L}. \end{cases} \quad (2)$$

The net differences between the original (without the UPFC) powers expressed in (2) and the new (with the UPFC) powers in (1) are the controllable active and reactive powers, P_C and Q_C by the transformerless UPFC, which can be expressed as

$$\begin{cases} P_C = \frac{V_CV_R}{X_L}\sin(\delta_0-\delta) \\ Q_C = -\frac{V_CV_R}{X_L}\cos(\delta_0-\delta). \end{cases} \quad (3)$$

Therefore, we can rewrite (1) as

$$\begin{aligned} P+jQ = &\underbrace{\left(-\frac{V_{S0}V_R}{X_L}\sin\delta_0\right)}_{P_0}+\underbrace{\frac{V_CV_R}{X_L}\sin(\delta_0-\delta)}_{P_C} \\ &+j\underbrace{\left(\frac{V_{S0}V_R\cos\delta_0-V_R^2}{X_L}\right)}_{Q_0}-\underbrace{\frac{V_CV_R}{X_L}\cos(\delta_0-\delta)}_{Q_C}. \end{aligned} \quad (4)$$

Because both amplitude V_C and phase angle δ of the UPFC injected voltage $\overrightarrow{V}_C$ can be any values as commanded, the new UPFC provides a full controllable range of $(-V_CV_R/X_L)$ to $(+V_CV_R/X_L)$for both active and reactive powers, P_C and Q_C, which are advantageously independent of the original sending-end voltage and phase angle δ_0. In summary, (1)–(4) indicate that the new transformerless UPFC has the same functionality as the conventional UPFC.

First, the series CMI voltage $\overrightarrow{V}_C$ is injected according to transmission line active/reactive power command, which can be calculated from (3)

$$\overrightarrow{V}_C = V_C\angle\delta = \frac{X_L}{V_R}\sqrt{P_C^2+Q_C^2}\angle\left(\delta_0-\arctan\left(\frac{P_C}{Q_C}\right)\right). \quad (5)$$

Once the series CMI injected voltage $\overrightarrow{V}_C$ is decided by (5), the new sending-end voltage $\overrightarrow{V}_S$ and the transmission line current will be decided accordingly

$$\overrightarrow{V}_S = V_S\angle\delta_S = \overrightarrow{V}_{s0}-\overrightarrow{V}_C \quad (6)$$

where

$$\begin{cases} V_S = \sqrt{(V_{S0}-V_C\cos\delta)^2+(V_C\sin\delta)^2} \\ \delta_S = \arctan\left(\frac{-V_C\sin\delta}{V_{S0}-V_C\cos\delta}\right) \end{cases} \quad (7)$$

and $\vec{I}_L = I_L\angle\rho$, where

$$\begin{cases} I_L = \frac{\sqrt{(V_C\sin\delta+V_R\sin\delta_0)^2+(V_{S0}-V_C\cos\delta-V_R\cos\delta_0)^2}}{X_L} \\ \rho = \arctan\left(\frac{V_{S0}-V_C\cos\delta-V_R\cos\delta_0}{V_C\sin\delta+V_R\sin\delta_0}\right). \end{cases} \quad (8)$$

Next, the shunt CMI injects current $\vec{I}_P$ to decouple the series CMI current $\vec{I}_C$ from the line current $\vec{I}_L$. In such a way, zero active power exchange to both series and shunt CMIs can be achieved, making it possible to apply the CMI with floating capacitors to the proposed transformerless UPFC. Therefore, we have

$$\begin{cases} P_{se} = \overrightarrow{V}_C\cdot\vec{I}_C = 0 \\ P_{sh} = \overrightarrow{V}_S\cdot\vec{I}_P = 0. \end{cases} \quad (9)$$

It means the series CMI current $\vec{I}_C$ and the shunt CMI current $\vec{I}_P$ need to be perpendicular to their voltages $\overrightarrow{V}_C$ and $\overrightarrow{V}_S$, respectively, as illustrated in Fig. 3. With the geometrical relationship of the voltages and currents in Fig. 3, the shunt CMI output current can be calculated as

$$\vec{I}_P = I_P\angle\theta_{Ip} \quad (10)$$

where

$$\begin{cases} I_P = I_L\left(\frac{\cos(\rho-\delta_S)}{\tan(\delta-\delta_s)}-\sin(\rho-\delta_S)\right) \\ \theta_{Ip} = 90+\delta_S. \end{cases} \quad (11)$$

In summary, there are two critical steps for the operation of UPFC: 1) calculation of injected voltage $\overrightarrow{V}_C$ for series CMI according to active/reactive power command over the transmission line expressed in (5), and 2) calculation of injected current $\vec{I}_P$ for shunt CMI from (10) and (11) to guarantee zero active power into both series and shunt CMIs.

III. Fundamental Frequency Modulation (FFM) for CMIs

Before embarking on development of UPFC control, the modulation strategy for CMIs is introduced first. In general, the modulation for CMIs can be classed into two main categories: 1) FFM [20]–[22], [24], [27], [29] and 2) carrier-based high-frequency pulse width modulation (PWM) [23], [30]–[34]. Compared to the carrier-based high-frequency PWM, the FFM has much lower switching loss, making it attractive for the transmission-level UPFC and other high-voltage high-power applications. The FFM has been investigated for many years, however, most studies focused on the FFM optimization with low number of modules (e.g., four to five) and the steady-state

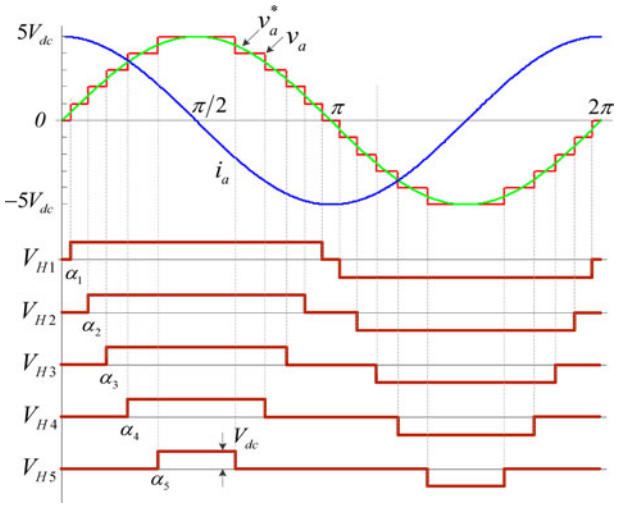

Fig. 4. Operation principle of FFM.

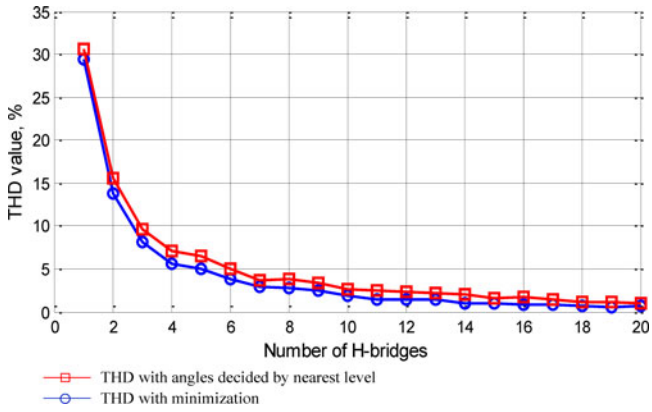

Fig. 5. Minimum THD versus number of H-bridge modules.

THD minimization. In this paper, FFM will be designed with high number of modules. Specifically, switching angles will be optimized for all ten series H-bridge modules and 20 shunt H-bridge modules to achieve extremely low THD. Furthermore, it will also demonstrate that CMIs with FFM can also achieve fast dynamic response, e.g., 8 ms.

A. *Optimization of Switching Angles for Minimum THD*

Fig. 4 shows the operation principle of traditional FFM, where phase *a* output voltage of an 11-level CMI is shown as an example. A stair-case voltage waveform, V_a could be synthesized when each of five H-bridge modules generates a quasi-square wave, $V_{H1}, V_{H2}, \ldots, V_{H5}$. Each H-bridge has the identical dc-link voltage $V_{\rm dc}$ for the modular design consideration. Different approaches have been studied in [20]–[22], [35], [36] to decide the switching angles of H-bridge modules for selected harmonic elimination or minimum THD. However, these papers mostly focused on low number (less than five) of H-bridge modules. In this paper, switches angles will be optimized for minimum THD with the high number of H-bridge modules for the transformerless UPFC (ten for series CMI and 20 for shunt CMI as given in Table I).

The Fourier series expansion of the CMI output voltage shown in Fig. 4 is

$$V_a(\omega t) = \sum_{n=1}^{\infty} V_{an} \cdot \sin(n\omega t),$$

$$V_{an} = \begin{cases} \dfrac{4}{n\pi} \displaystyle\sum_{k=1}^{s} V_{dc} \cdot \cos(n\alpha_k), & \text{for odd } n \\ 0, & \text{for even } n \end{cases} \tag{12}$$

where *n* is harmonic number, *s* is the total number of H-bridge modules, and α_k represents the switching angle for the kth H-bridge module. For a three-phase system, the THD of line voltage instead of phase voltage is of interest. Therefore, all triplen harmonics will be ignored for voltage THD calculation, which then can be expressed as

$$\text{THD} = \frac{1}{V_{a1}} \sqrt{\sum_{n=5,7,11,\ldots}^{\infty} V_{an}^2}. \tag{13}$$

Basically, (13) gives an objective function to be minimized, with the following two constraints:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 \ldots < \alpha_s < \frac{\pi}{2} \tag{14}$$

and

$$V_{a1} = \frac{4}{\pi} \sum_{k=1}^{s} V_{dc} \cos(\alpha_k). \tag{15}$$

(14) indicates that the switching angles from first H-bridge module to last H-bridge module gradually increase, while the corresponding duty cycles (pulse width) of output voltage would inversely decrease. In (15), V_{a1} is the desired fundamental voltage, which is equal to the reference voltage $V_{a1} = V_a^*$. With the Matlab optimization toolbox, we can get the minimum THD with above two constraints in (14) and (15). The corresponding results have been shown in Fig. 5. For a comparison purpose, the line voltage THD with angles decided by nearest level is also given [37]. From Fig. 5, it clearly shows that the THD is decreased with the increase of number of H-bridge modules *s*. When $s \geq 15$, the minimum THD will be smaller than 1% even without any additional filters.

In addition, an alternative optimization of FFM could be the "minimum weighted total harmonics distortion (WTHD)." The WTHD achieves the minimum current THD for inductive loads (i.e., directly optimized for best power quality), which is preferred for application where current distortion is of interest. In such a case, the objective function in (13) should be changed to

$$\text{WTHD} = \frac{1}{V_{a1}} \sqrt{\sum_{n=5,7,11,\ldots}^{\infty} (V_{an}/n)^2}. \tag{16}$$

As shown in Table I, for the 13.8-kV/2-MVA system, the number of H-bridges for shunt CMI is ten and the number of H-bridges for series CMI is 20. Fig. 6 shows FFM with total 20 H-bridges, (a) output voltage and current and (b) output voltage of

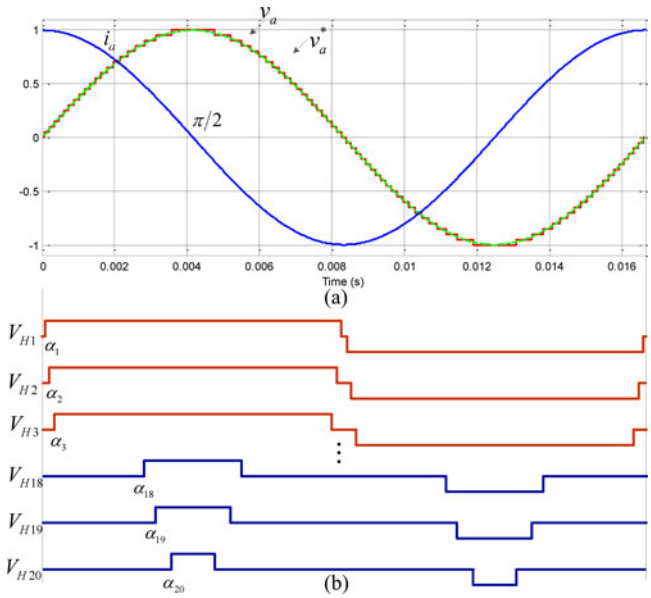

Fig. 6. FFM with total 20 H-bridges. (a) Output voltage and current (41 levels) and (b) output voltage of each H-bridge.

each H-bridge, where modulation index $\mathrm{MI} = 1$ in this case. MI is defined as peak phase voltage divided by $(s * V_{\mathrm{dc}})$. With total 20 H-bridges, the CMI output phase voltage can reach up to 41 levels. The output voltage is very close to sinusoidal waveform, achieving extremely low THD ($= 0.85\%$). The corresponding optimized switching angles for this case are given in Table II.

In summary, compared to carrier-based high-frequency PWM scheme, the CMIs with FFM have the following features:

1) FFM has much lower switching loss, thus higher efficiency;
2) with high number of H-bridge modules, output voltage could be very close to sinusoidal, and extremely low THD (e.g., 0.85%) could be achieved without any extra filters;
3) it is notable that FFM does not actually mean slow dynamic response. With high-frequency sampling, FFM can also achieve fast dynamic response, e.g., <10 ms, which will be discussed and experimentally verified in the next section.

B. Analysis of Capacitor Charge of H-Bridges

Capacitor charge of H-bridges will be studied based on two layers: 1) first layer is overall capacitor charge, meaning the total capacitor charge of all H-bridges of any one of three phases; 2) the other layer is individual capacitor charge, meaning the capacitor charge of each H-bridge.

In previous analysis, the CMI output voltage is expected to lead or lag the output current by 90°, to achieve zero active power flow from ac side into dc capacitors. In practice, the dc capacitor voltage cannot be maintained due to the power loss of switching devices and capacitors. Still take phase *a* of a CMI as an example, the overall active power flow of this phase from ac side into dc capacitors can be expressed as

$$P_a = V_o I_o \cdot \cos(\theta) \tag{17}$$

where V_o and I_o are rms values of CMI output phase voltage and current, respectively, and θ is the phase angle between output voltage and current. As mentioned before, if θ is exact 90°, then $P_o = 0$. No any active power will flow from ac side to dc side to charge dc capacitors. Obviously, in this case, no matter overall capacitor charge or individual capacitor charge is zero. However, if the phase angle θ is smaller than 90°, denoted as$(90^\circ - \Delta\theta)$, the overall dc capacitor voltage could be balanced if

$$P_a = V_o I_o \cdot \cos(90 - \Delta\theta) = V_o I_o \sin(\Delta\theta) = P_{\mathrm{loss}} \tag{18}$$

where P_{loss} is the total power loss of switching devices and capacitors of one phase. Therefore, the CMI should be controlled to absorb small amount of active power in order to maintain the desired dc-link voltage.

On the other side, with the shifted phase angle $\Delta\theta$, the individual capacitor charge for kth H-bridge, C_k over one fundamental period is

$$\begin{aligned} C_k &= \int i_{\mathrm{dc}} dt = \frac{2}{\omega} \cdot \int_{\alpha_k - \Delta\theta}^{\pi - \alpha_k - \Delta\theta} \sqrt{2} I_o \cos(\theta) d\theta \\ &= \frac{4}{\omega} \sqrt{2} I_o \cos(\alpha_k) \sin(\Delta\theta) \end{aligned} \tag{19}$$

where $k = 1, 2, \ldots, s$. In (19), the entire modules in the same phase will have same load current I_o and phase angle shift $\Delta\theta$. (19) indicates the quite different individual capacitor charge due to the unequal duty cycles of H-bridge modules. Fig. 7 illustrates the capacitor charges of 20 shunt H bridges with corresponding switching angles given in Table II. When the same load current go through all these 20 H bridges, dc capacitor of each H bridge will be charged differently.

One important point here is, the smaller switching angle (corresponding to larger duty cycle) an H-bridge module has, the more capacitor charge it will get.

IV. Power Flow and DC-Link Voltage Control of Transformerless UPFC

A. Dynamic Models of UPFC System

The equations derived from the phasor diagram in Section II are limited to steady-state operation analysis. In order to design the vector-oriented control for the proposed transformerless UPFC with considering both steady-state and dynamic performance, the dynamic modules are necessary. The models are based on synchronous (*dq*) reference frame. The phase angle of original sending-end voltage V_{s0} is obtained from a digital phase-locked loop, which is used for *abc* to *dq* transformation.

The dynamic models for the whole system shown in Fig. 2(a) will be divided into several parts. First, we can get the dynamic model from the new sending-end bus to receiving-end bus

$$\begin{cases} V_{sd} = R_L i_{Ld} + L_L \frac{di_{Ld}}{dt} - \omega L_L i_{Lq} + V_{Rd} \\ V_{sq} = R_L i_{Lq} + L_L \frac{di_{Lq}}{dt} + \omega L_L i_{Ld} + V_{Rq}. \end{cases} \tag{20}$$

Since the new sending-end voltage v_s is equal to original sending-end voltage v_{s0} minus series CMI injected voltage v_c,

TABLE II
SWITCHING ANGLES FOR THE CASE MI = 1

Switching Angles	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}
Value (rad)	0.0276	0.0745	0.1244	0.1828	0.2194	0.2657	0.3380	0.3952	0.4438	0.4947
Switching Angles	α_{11}	α_{12}	α_{13}	α_{14}	α_{15}	α_{16}	α_{17}	α_{18}	α_{19}	α_{20}
Value (rad)	0.5535	0.6213	0.6897	0.7373	0.7972	0.8900	0.9689	1.0649	1.1849	1.3550

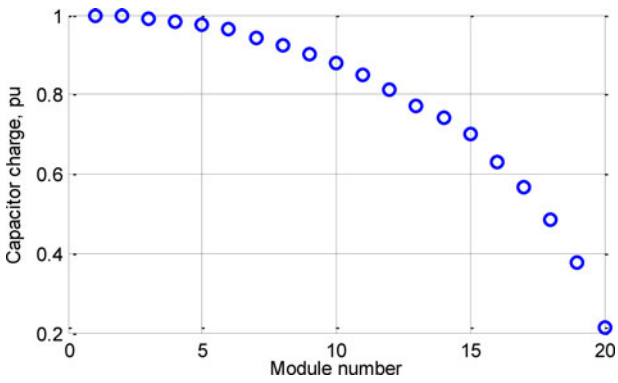

Fig. 7. Capacitor charge of 20 H-bridge modules with FFM.

thus we have

$$\begin{cases} V_{Cd} = V_{S0d} - V_{Sd} \\ V_{Cq} = V_{S0q} - V_{Sq}. \end{cases} \tag{21}$$

Furthermore, the model from the new sending-end to shunt CMI is

$$\begin{cases} V_{sd} = R_s i_{Pd} + L_s \frac{di_{Pd}}{dt} - \omega L_s i_{Pq} + V_{pd} \\ V_{sq} = R_s i_{Pq} + L_s \frac{di_{Pq}}{dt} + \omega L_s i_{Pd} + V_{pq}. \end{cases} \tag{22}$$

B. Power Flow and Overall DC Voltage Control

It is desired to design a control system, which can independently regulate the active power P and reactive Q in the line, at the same time, maintain the capacitor voltages of both CMIs at the given value. Fig. 8(a) shows the overall control system, which is divided into three stages, i.e., stage I to stage III.

Stage I: the calculation from P^*/Q^* to $\overrightarrow{V_{C0}^*}$ and $\overrightarrow{I_{p0}^*}$. As mentioned before, the $\overrightarrow{V_{C0}^*}$is the voltage reference for series CMI, which is generated according to the transmission line power command as given in (5), while $\overrightarrow{I_{p0}^*}$ is current reference for shunt CMI, which is used to keep zero active power for both CMIs as given in (10), (11). Note that instead of calculating $\overrightarrow{V_{C0}^*}$ directly from (5), an alternative way is shown in Fig. 8(b). Here, the line current reference $I_{Ld}^*/I_{Lq}^*$is calculated out of the P^*/Q^* reference, then the d- and q-axis components of series voltage V_{C0d}^*, V_{C0q}^* are calculated according to (23), where the dynamic model of (20) is included. The line current is controlled in a way of decoupling feedforward control, thus better line current dynamic response could be achieved

$$\begin{cases} V_{C0d}^* = V_{S0d} - V_{Sd}^* = \\ \quad V_{S0d} - \left(R_L I_{Ld}^* + L_L \frac{dI_{Ld}^*}{dt} - \omega L_L I_{Lq}^* + V_{Rd} \right) \\ V_{C0q}^* = V_{S0q} - V_{Sq}^* = \\ \quad V_{S0q} - \left(R_L I_{Lq}^* + L_L \frac{dI_{Lq}^*}{dt} + \omega L_L I_{Ld}^* + V_{Rq} \right). \end{cases} \tag{23}$$

Stage II: overall dc-link voltage regulation. With the $\overrightarrow{V_{C0}^*}$ and $\overrightarrow{I_{p0}^*}$ given in stage I, the dc-link voltage cannot be maintained due to the following three main reasons: 1) the CMIs always have a power loss, 2) the calculation error caused by the parameter deviations, 3) the error between reference and actual output. In order to control dc-link voltage with better robustness, two variables $\overrightarrow{\Delta V_C}$ and $\overrightarrow{\Delta I_P}$ were introduced for the independent dc-link voltage regulation of series CMI and shunt CMI, respectively, as shown in Fig. 8(a). In this figure, $V_{\mathrm{dc\_}sh}^*$ and $V_{\mathrm{dc\_}se}^*$ are dc voltage references for shunt and series CMIs, respectively; $V_{\mathrm{dc\_}sh}$ and $V_{\mathrm{dc\_}se}$ are the averaged dc feedback of shunt and series CMIs, respectively. For the series CMI, P_{se} is the output of overall dc-link voltage regulation loop, R_{se} is then calculated by dividing P_{se} by I_C^2 (square of rms value of series CMI current), finally $\overrightarrow{\Delta V_C}$ is the product of R_{se} and series CMI current $\overrightarrow{I_C}$. Obviously, the introduced $\overrightarrow{\Delta V_C}$ is always in phase with series CMI $\overrightarrow{I_C}$, which can be regarded as *active-voltage* component. Basically, R_{se} is the equivalent resistance of series CMI, and the dc-link can be balanced when P_{se} is equal to P_{loss} (total power loss of series CMI). For the shunt CMI, $\overrightarrow{\Delta I_P}$ is introduced for the dc-link voltage control in a similar way.

The mathematical model and detailed parameters design for the overall dc voltage control can be found in [31]. Usually, the CMI should be considered as three single-phase inverters, therefore, the dc capacitor voltage will contain the 2ω (two times of the fundamental frequency) component. To keep the average dc track the command without being affected by the 2ω ripple, the bandwidth of current control loop and dc voltage control loop is designed to be differential. For example, the current control loop has been designed to have fast dynamic response (e.g., half cycle, 8 ms), while dc voltage control loop has been designed to have much slower dynamic response (e.g., ten cycles). In this way, the 2ω ripple can be suppressed in the voltage control loop.

Stage III: voltage and current generation for series and shunt CMI, respectively. For series CMI, output voltage could be directly generated from the reference $\overrightarrow{V_C^*}$ by FFM. While for shunt CMI, decoupling feedback current control is used to control output current to follow the reference current $\overrightarrow{I_P^*}$, as shown in Fig. 8(c) [22].

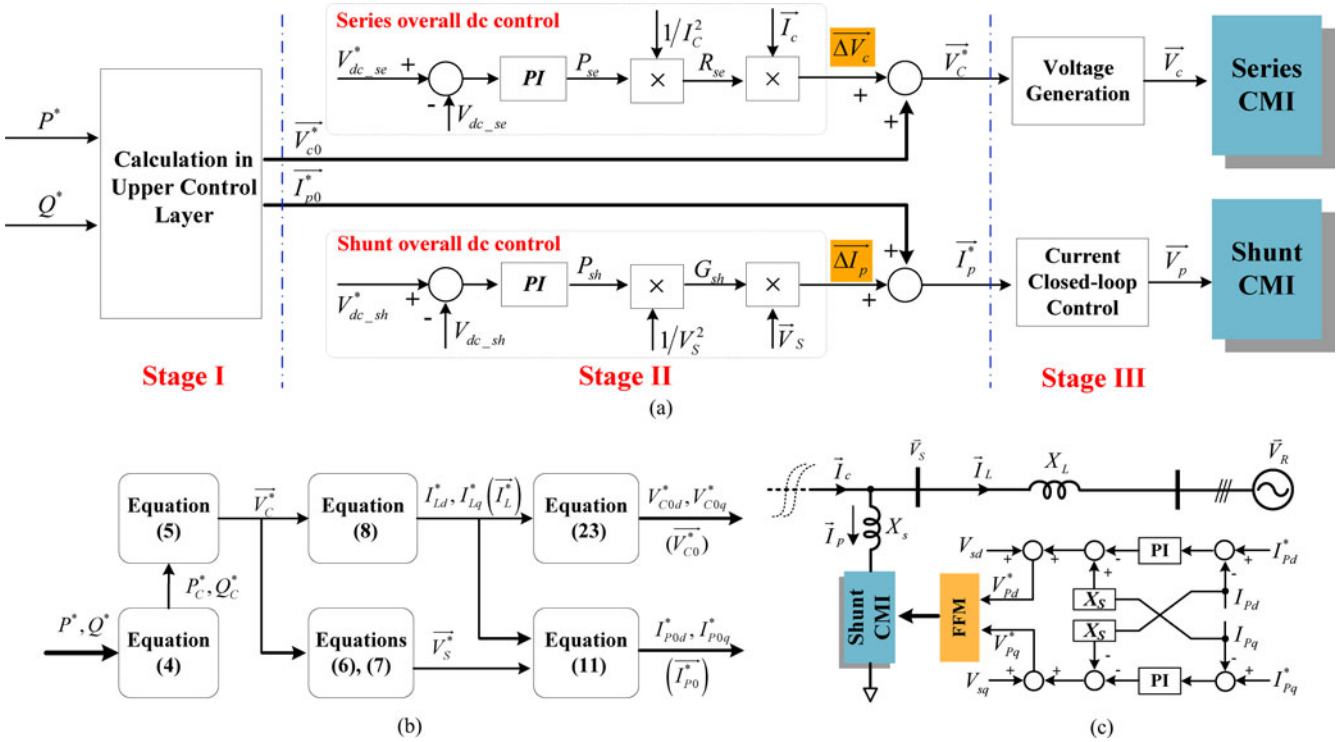

Fig. 8. Control system for transformerless UPFC. (a) Overall control diagram for both power flow and dc capacitor voltage control, (b) detailed calculation from P^*/Q^* to $\overrightarrow{V^*_{C0}}$ and $\overrightarrow{I^*_{p0}}$, and (c) current closed-loop control for shunt CMI.

C. Individual DC Control and Phase Balance Control

Usually, the dc capacitor voltage balance control for CMIs adopts hierarchical control structure, e.g., an outer control loop and an inner control loop. The outer loop regulates the overall active power flowing to all H-bridge modules of any one of three phases, while the inner loop distributes power flowing equally to each individual H-bridge module [22]. As we discussed in Section III, one fact is that the capacitor charge of individual H-bridge will be unequal due to the unequal duty cycles of each H-bridge by FFM. The smaller switching angle (corresponding to larger duty cycle) an H-bridge module has, the more capacitor charge it will get. Besides the overall dc capacitor voltage control present above, it is necessary to have the individual dc capacitor voltage control for the charge balance between the modules in the same phase. This is implemented by pulse swapping every fundamental cycle [29]. Fig. 9 illustrates the pulse swapping from one fundamental cycle to the next fundamental cycle, taking ten H-bridge modules as an example. In the first fundamental cycle, the optimized ten switching angles are distributed to ten H-bridge modules in a special sequence. After one cycle, the switching angles for the H-bridge modules will be swapped as illustrated in Fig. 9. If we take a look at the switching angles for each of the ten modules, it would be in an order of $\alpha_1, \alpha_{10}, \alpha_2, \alpha_9, \alpha_3, \alpha_8, \alpha_4, \alpha_7, \alpha_5, \alpha_6, \alpha_1, \ldots$ for the successive fundamental cycles. Since smaller switching angle (corresponding to larger duty cycle) of an H-bridge module results in more capacitor charge. Therefore, such an order for the H-bridge module would result in better charge/discharge balance, leading to lower dc-link voltage ripple.

Even with both overall and individual dc capacitor voltage control described above, it is still possible to have the dc capacitor voltage unbalance between the three phases. Physically, the shunt CMI or series CMI may have different power loss between the three phases. If same P_{sh}/P_{se} from overall dc voltage regulator is applied to all three phases of shunt/series CMI as shown in Fig. 8(a), the mismatch between the absorbed active power and the power loss would cause the voltage unbalance. One simple solution to this problem is to change the overall dc voltage control in Fig. 8(a) from one three-phase integrated controller to three separated controllers as shown in Fig. 10, where $V_{\mathrm{dc\_sea}}$, $V_{\mathrm{dc\_seb}}$, and $V_{\mathrm{dc\_sec}}$ are dc capacitor voltage feedback of phase a, b, and c, respectively; P_{se_a}, P_{se_b}, P_{se_c} are active power commands, which are used to compensate the power loss of each phase; i_{c_a}, i_{c_b} and i_{c_c} are instantaneous currents of each phase of series CMIs; Δv_{c_a}, Δv_{c_b}, Δv_{c_c} are generated as the *active-voltage* components, which are in phase with current i_{c_a}, i_{c_b} and i_{c_c}, respectively. In a three-phase well balanced system, P_{se_a}, P_{se_b}, P_{se_c} will be close to each other, indicating the same active power is needed to compensate the power loss of each phase; while in a system with different power losses between three phases, the separated dc regulators will output different value of P_{se_a}, P_{se_b} and P_{se_c} to guarantee the balanced dc capacitor voltage. It is notable that the value of P_{se_a}, P_{se_b} and P_{se_c} are relatively small when compared to the total UPFC system rating. Similarly, from Fig. 8(a) we

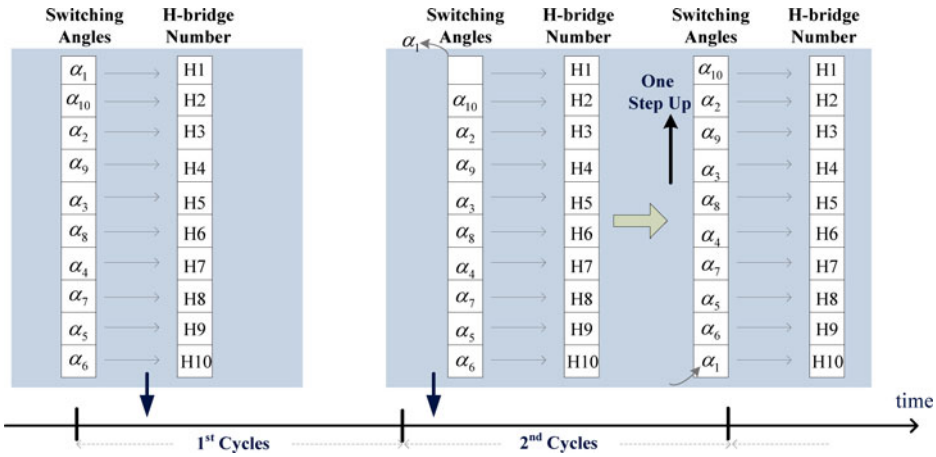

Fig. 9. Illustration of pulse swapping from one fundamental cycle to next fundamental cycle.

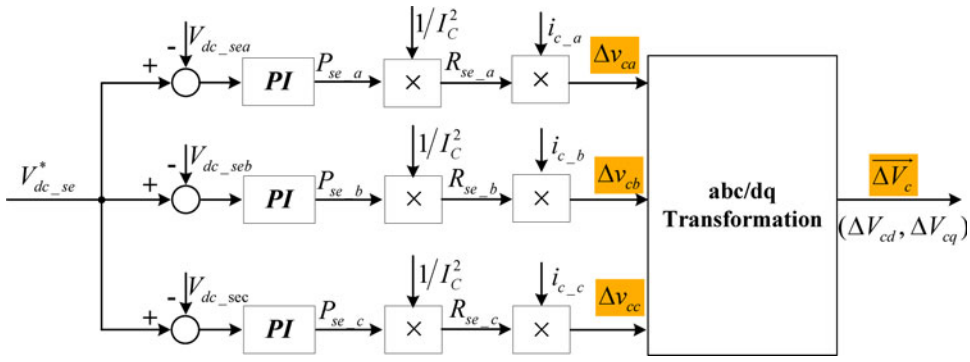

Fig. 10. Three-phase separated overall dc voltage control for series CMI, considering capacitor-voltage unbalance between the three phases.

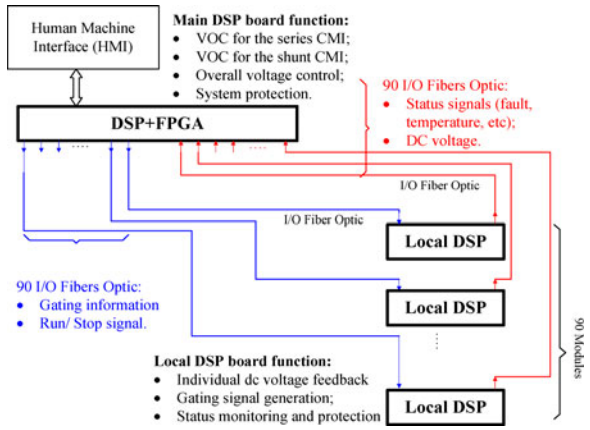

Fig. 11. Architecture of the control system.

can derive the corresponding three-phase separated overall dc voltage control for shunt CMI.

D. Implementation and Architecture of Control System

The control system for the CMIs based UPFC consists of a main control board for the system level control and local control boards for module level control as shown in Fig. 11. The main control board has a state-of-the-art floating-point DSP and FPGA, which will be used for implementation of overall system control as shown in Fig. 8(a), system level protection, as well as communications with local control board and human machine interface. In the designed main control board, total $13 * 8 = 104$ pairs of fiber-optic transmitters and receivers are available, which provides enough channels to communicate with total 90 H-bridge modules (30 series H-bridge modules, 60 shunt H-bridge modules). The main task of the local control board is to implement individual dc voltage feedback, fundamental switching signals generation, local protection and communication with main control board. The universal asynchronous receiver transmitter communication is used between the main control board and local control board. High communication speed with baud rate 500 k is used to support the high-frequency sampling ≥ 1 kHz.

V. Experimental Results

To validate the functionality of the transformerless UPFC system with proposed modulation and control algorithm, a 4160-V test setup has been developed as shown in Fig. 12(a), and the main system parameters for this test setup are given in Table III. Fig. 12(b) shows the corresponding equivalent circuit of this test setup, which is consistent with the circuit configuration shown in Fig. 2(a). In Fig. 12(b), the equivalent receiving-end voltage

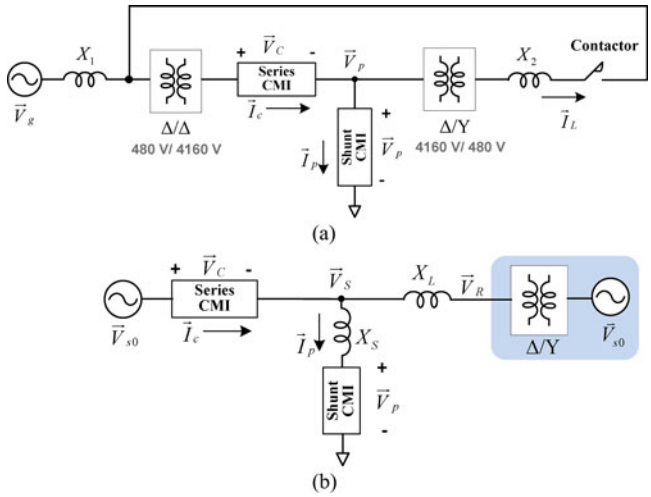

Fig. 12. 4160-V transformerless UPFC test setup. (a) Circuit configuration and (b) corresponding equivalent circuit.

TABLE III
SYSTEM PARAMETERS FOR TEST SETUP

Parameter	Value
Grid voltage (low voltage side) V_g	480 V
Rated frequency	60 Hz
Sampling frequency	2.5 kHz
V_{dc} of each shunt H-bridge	600 V
V_{dc} of each series H-bridge	600 V
No. of H-bridges per phase (Shunt)	6
No. of H-bridges per phase (Series)	3
Transformer 1 (Δ/Δ)	480 V/ 4160 V, 75 kVA
Transformer 2 (Y/Δ)	480 V/ 4160 V, 75 kVA
Dc capacitance of each H-bridge	2350 μF
Rated line current	10 A
Reactor X_1	2.5 mH
Reactor X_2	3.2 mH
Leakage inductance of transformer 1 (Δ/Δ)	35 mH (6% p.u.)
Leakage inductance of transformer 2 (Y/Δ)	35 mH (6% p.u.)
Equivalent line inductance X_L	0.31 H (50% p.u.)
Equivalent shunt filter inductance X_S	0.22 H (36% p.u.)

$\overrightarrow{V}_R$ has same amplitude as original sending-end voltage $\overrightarrow{V}_{S0}$, but 30° phase lagging. This 30° phase lagging is introduced by transformer 2 with Y/Δ configuration (Y/Δ, 480 V/4160 V). The basic functions of the UPFC (i.e., voltage regulation, line impedance compensation, phase shifting and simultaneous control of voltage, impedance and angle) have been tested based on this setup. Some experimental results are given in this section.

A. UPFC Operation - Phase Shifting

The UPFC can function as a perfect phase angle regulator, which achieves the desired phase shift (leading or lagging) of the original sending-end voltage without any change in magnitude. Three operating points with different shifted phases are considered as shown in Fig. 13(a) case A1: 30°, (b) case A2: 15°, and (c) case A3: 0°. All three phase shifting cases (case A1 to case A3) have been tested and corresponding test results are

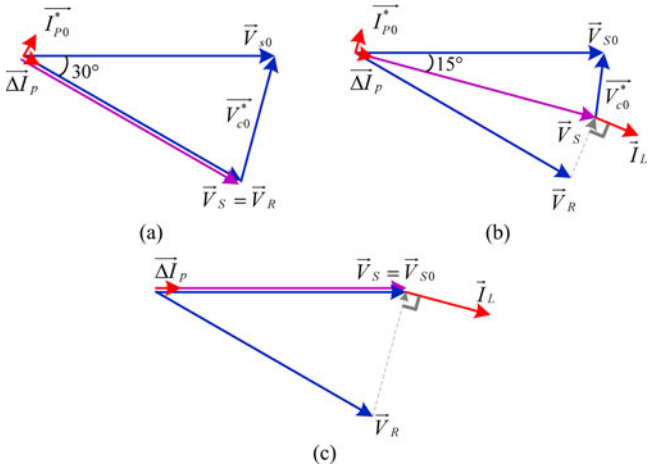

Fig. 13. UPFC operating points with different phase shifting: (a) case A1: 30°, (b) case A2: 15°, and (c) case A3: 0°.

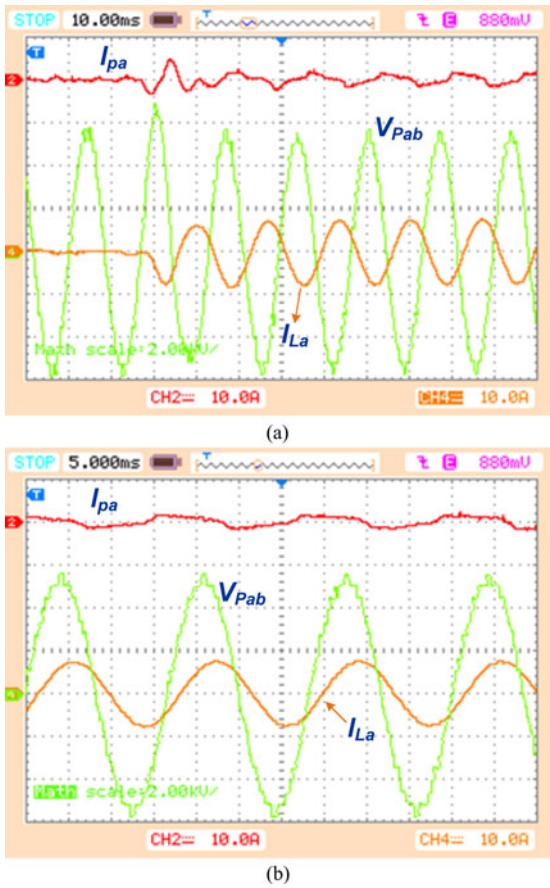

Fig. 14. Experimental waveforms of UPFC operating from case A1 to case A2 (phase shifting 30° to 15°): (a) shunt CMI line voltage V_{Pab}, shunt CMI phase current I_{Pa}, and line current I_{La}, and (b) the zoomed in waveforms.

shown in Figs. 14–17. Some discussions about the test results are given as follows:

1) Fig. 14 shows the experimental waveforms of UPFC operating from case A1 to case A2 (Phase shifting 30° to 15°). As mentioned before, in the test setup, there is already 30° phase difference between the original sending-end

voltage $\overrightarrow{V}_{S0}$ and the receiving-end voltage $\overrightarrow{V}_R$. For case A1, series CMI voltage $\overrightarrow{V}_C$ is injected to shift $\overrightarrow{V}_{S0}$ by 30° lagging, as a result, $\overrightarrow{V}_S = \overrightarrow{V}_R$. In this case, UPFC is used to compensate voltage difference caused by transformer 30° phase shift. Therefore, the resulting line current in this case is almost zero. While for case A2, new sending-end voltage $\overrightarrow{V}_S$ is shifted from $\overrightarrow{V}_{S0}$ by 15°, therefore, there is 15° phase difference between $\overrightarrow{V}_S$ and $\overrightarrow{V}_R$. This will result in about 7-A (peak value) line current. Fig. 14(a) and (b) shows the experimental waveforms of shunt current I_{Pa}, line current I_{La}, and shunt CMI output line voltage V_{pab}. When the phase voltage of shunt CMI were generated by FFM with optimized switching angles for low THD, the line voltage would have even lower THD due to absence of the triplen harmonics in a balanced three-phase system. From Fig. 14, it shows the line voltage is very close to sinusoidal without any extra filters. In addition, Fig. 14 also shows that the current smoothly and quickly raised from zero to 7 A, when the operating point is changed from case A1 to A2.

2) Similarly, the experimental waveforms of UPFC operating from case A2 to case A3 (Phase shifting 15° to 0°) are shown in Fig. 15. Fig. 15(a) shows the shunt CMI phase voltage V_{Pa}, V_{Pb} and line current I_{La}, I_{Lb}, I_{Lc}. The V_{pa} and V_{pb} are stair-case waveforms, which are generated by the FFM with optimized switching angles. Fig. 15(b) shows the line current I_{La} and shunt CMI line voltage V_{Pab}. For case A3, phase shifting is zero degree, indicating a system without compensation. Therefore, $\overrightarrow{V}_S$ is equal to $\overrightarrow{V}_{S0}$, and the phase angle between $\overrightarrow{V}_S$ and $\overrightarrow{V}_R$ is 30°. The resulting current amplitude in this case is 14 A.
3) Fig. 16 shows the measured dynamic response with operating point changing from case A2 to case A3, where the current amplitude would change from 7 to 14 A. Since the system dynamic model has been included in the control algorithm as shown in Fig. 8, the UPFC system has achieved fast dynamic response, with response time $<$ 10 ms. This dynamic performance is good enough for transmission-level power flow control.
4) Fig. 17 shows the experimental results of dc capacitor voltage of both series and shunt CMIs when operating from case A2 to case A3, where top three waveforms correspond to average dc voltage of each phase, and bottom one corresponds to average dc voltage of all three phases. During the transition, the dc link voltage almost kept constant, which means the dc link voltage can be controlled to follow the reference faithfully regardless of operating points.

B. UPFC Operation - Line Impedance Compensation

UPFC function of line impedance compensation is different from phase shifting, where the series CMI voltage $\overrightarrow{V}_C$ is injected in quadrature with the line current. Functionally it is similar to series capacitive or inductive line compensation attained by static synchronous series compensator. Fig. 18 shows three

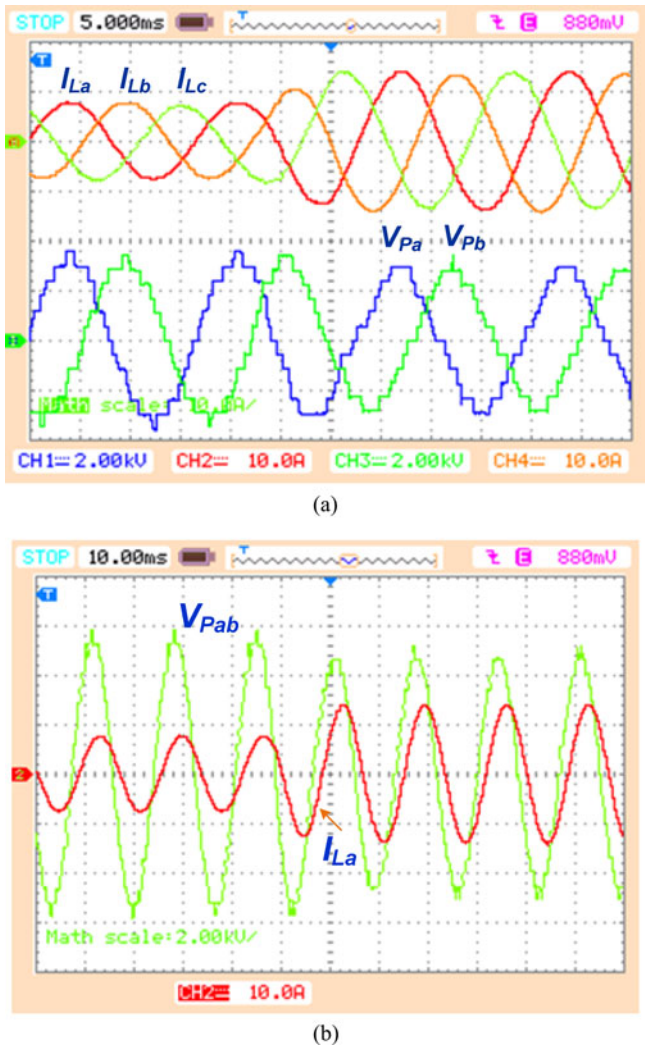

Fig. 15. Experimental waveforms of UPFC operating from case A2 to case A3 (phase shifting 15° to 0°): (a) shunt CMI phase voltage V_{Pa}, V_{Pb} and line current I_{La}, I_{Lb}, I_{Lc}, and (b) line current I_{La} and shunt CMI line voltage V_{Pab}.

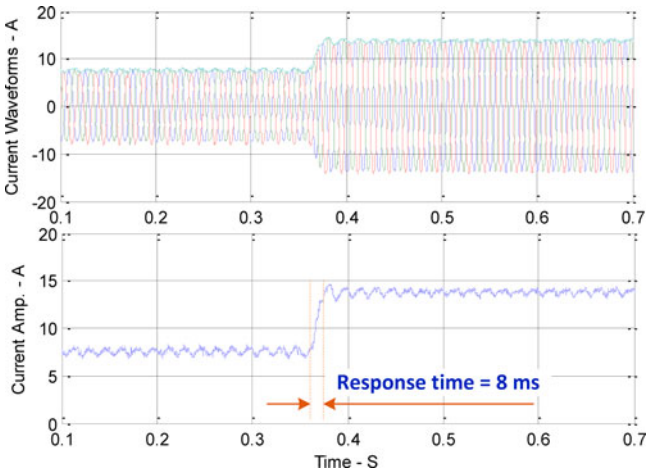

Fig. 16. Measured dynamic response with operating point changing from case A2 to case A3 (phase shifting 15° to 0°).

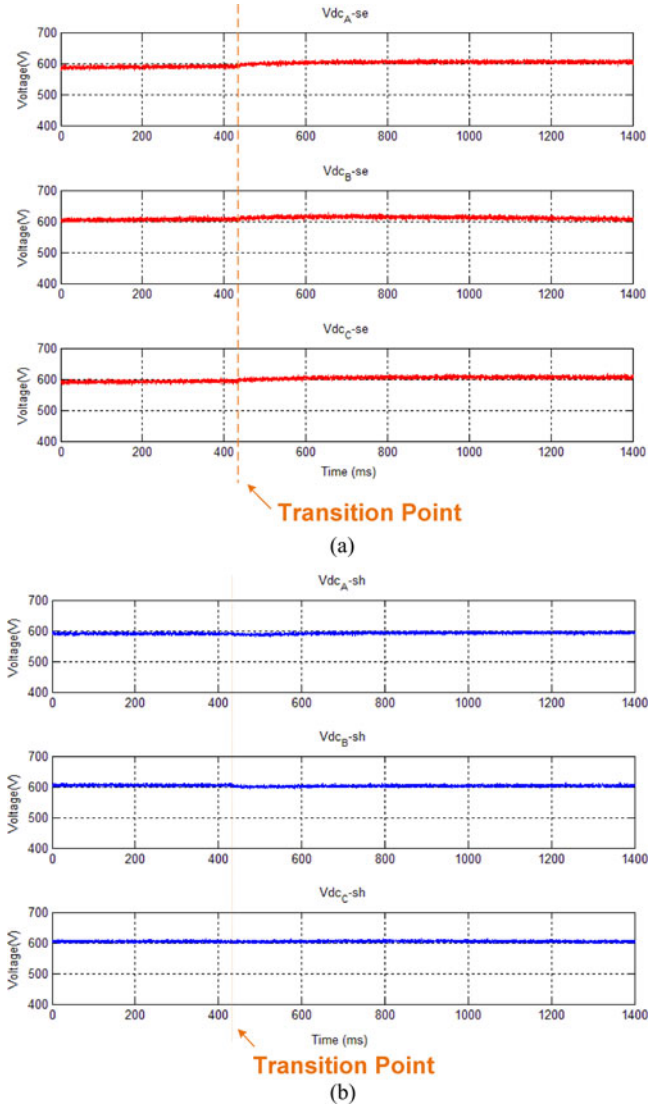

Fig. 17. Experimental results of dc capacitor voltage of series and shunt CMIs, from case A2 to case A3 (phase shifting 15° to 0°): (a) dc capacitor voltage of series CMI and (b) dc capacitor voltage of shunt CMI.

operation points with line impedance compensation, (a) case B1: original line impedance without compensation is equal to 0.5 p.u., (b) case B2: equivalent line impedance after compensation is equal to 1 p.u., and (c) case B3: equivalent line impedance after compensation is equal to infinity. For case B1 (same as case A3), system without compensation has 0.5 p.u. voltage between $\overrightarrow{V}_S$ and $\overrightarrow{V}_R$ (corresponding to 30° voltage difference). With the line impedance equal to 0.31 H (0.5 p.u.) given in Table III, the resulted line current is 1 p.u. (amplitude 14 A), which is the nominal current for transformer 1 and transformer 2 in the 4160-V test setup. Due to the current limitation of transformers, for case B2 and case B3, UPFC is purposely controlled to increase the line impedance. Nevertheless, the transformerless UPFC is also able to reduce the line impedance for higher line current (or higher *P*/*Q*).

Fig. 19 shows the experimental results of UPFC operation from case B1 to case B2, where the line impedance changed

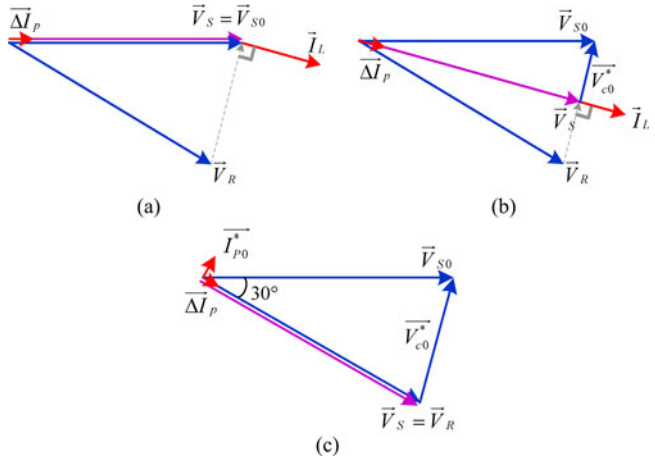

Fig. 18. UPFC operating points with line impedance compensation: (a) case B1: original line impedance without compensation = 0.5 p.u., (b) case B2: equivalent line impedance after compensation = 1 p.u., and (c) case B3: equivalent line impedance after compensation = ∞.

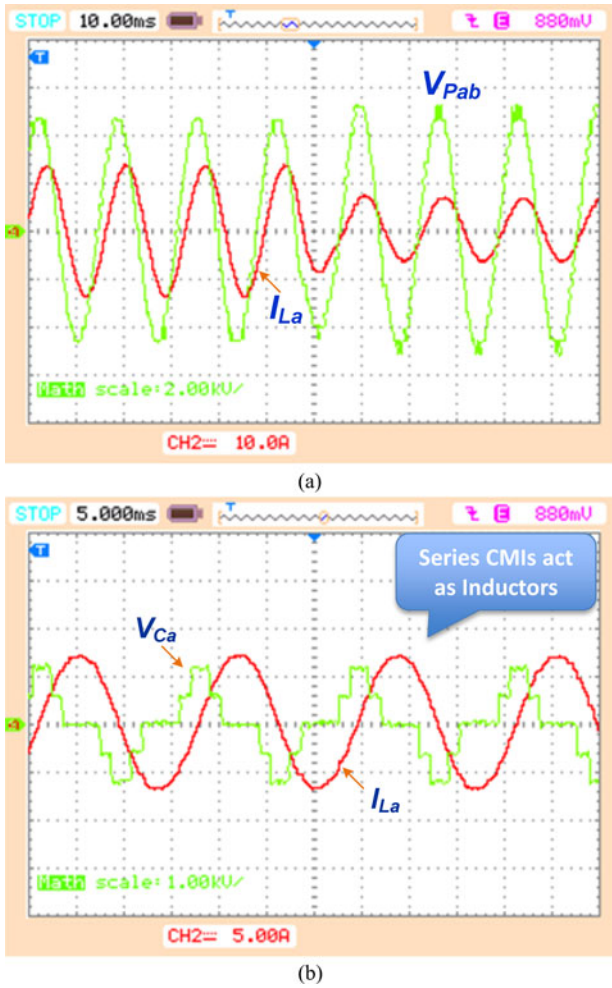

Fig. 19. Experimental waveforms of UPFC operating from case B1 to case B2 (line impedance from original 0.5 p.u. without compensation to 1 p.u. after compensation): (a) line current I_{La} and shunt CMI line voltage V_{Pab}, (b) line current I_{La} and series CMI phase voltage V_{Ca}.

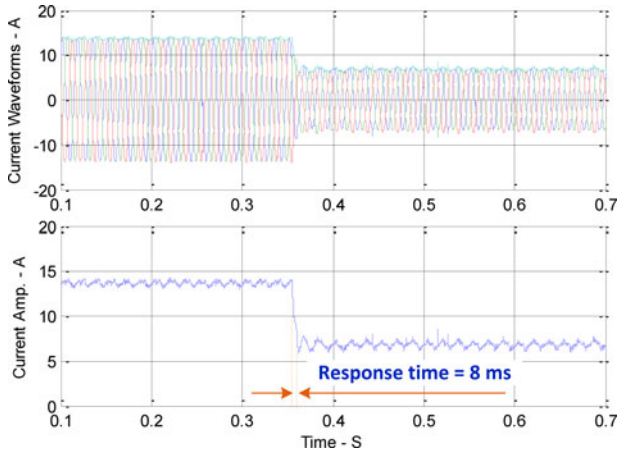

Fig. 20. Measured dynamic response with operating point changing from case B1 to case B2 (line impedance from original 0.5 p.u. without compensation to 1 p.u. after compensation).

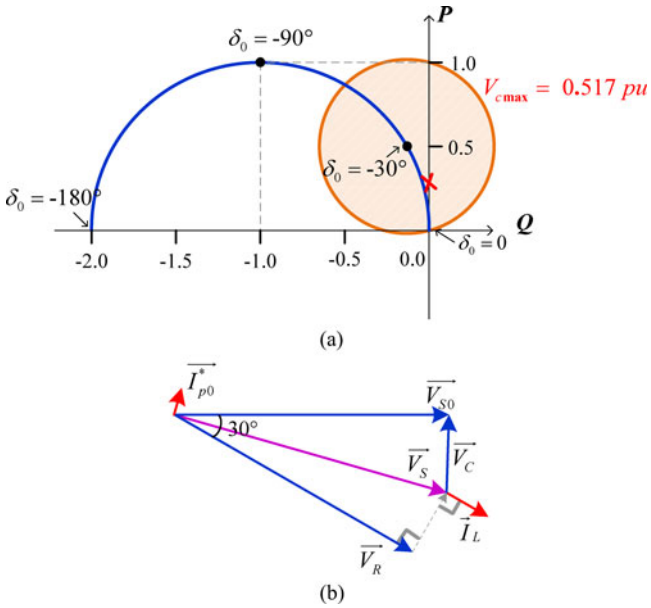

Fig. 21. Independent *P*/*Q* control: (a) control region of the attainable active power *P* and receiving-end reactive power *Q* with series CMI voltage = 0.517 p.u. and $\delta_0 = -30°$, (b) case C1: $P = 0.25$, $Q = 0$.

from original 0.5 p.u. without compensation to 1 p.u. after compensation. Fig. 19(a) shows the waveforms of shunt CMI phase voltage V_{Pa}, V_{Pb} and line current I_{La}, I_{Lb}, I_{Lc}, where the line current smoothly changed from 14 to 7 A (peak value) due to the doubled line impedance. Fig. 19(b) shows the waveforms of the series CMI injected voltage V_{Ca} and line current I_{La}. From this figure, we can see the line current I_{La} is lagging V_{Ca} by 90°, which means the series CMIs act as inductors. This is the reason that, after compensation, the line impedance is increased from 0.5 to 1 p.u. Fig. 20 shows the dynamic response with operating point changing from case B1 to case B2. The measured response time is about 8 ms.

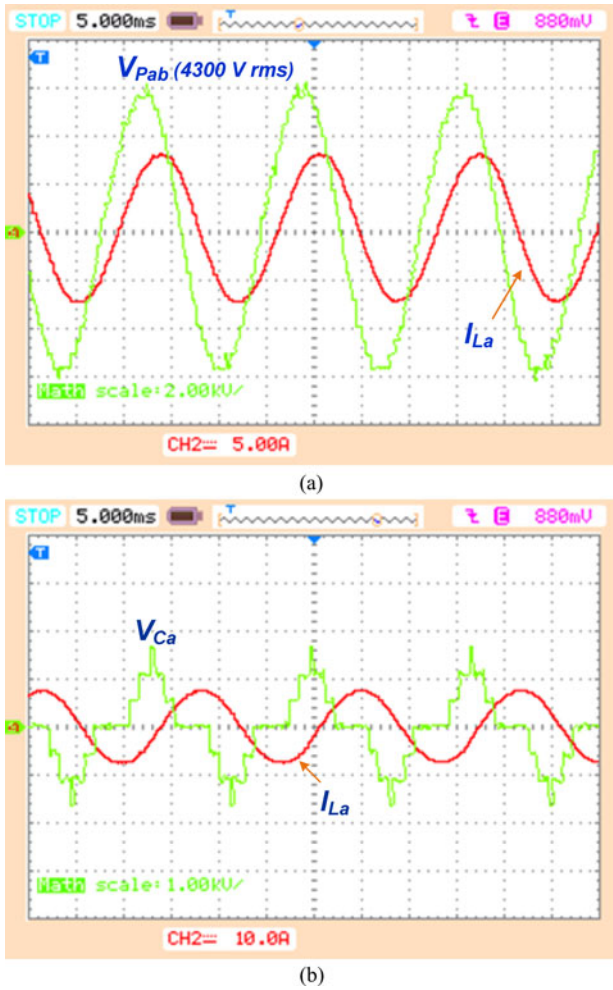

Fig. 22. Experimental waveforms of UPFC operation case C1: $P = 0.25$, $Q = 0$: (a) line current I_{La} and shunt CMI line voltage V_{Pab}, and (b) line current I_{La} and series CMI phase voltage V_{Ca}.

C. UPFC Operation - Independent P/Q Control

The functions of voltage regulation, phase shifting and line impedance compensation are from the standpoint of traditional power transmission control. Actually, the UPFC can simply control the magnitude and phase angle of the injected voltage in real time so as to maintain or vary the active and reactive power flow in the line to satisfy load demand and system operating conditions, i.e., independent *P*/*Q* control.

The blue curve in Fig. 21(a) shows the transmittable active power *P* and receiving-end reactive power *Q* versus receiving-end voltage phase angle δ_0 in the uncompensated system, where original sending-end voltage is oriented to 0°. The circle in Fig. 21(a) shows the control region of the attainable active power and receiving-end reactive power with series CMI voltage equal to 0.517 p.u. and phase angle δ_0 equal to $-30°$. In general, at any given δ_0, the transmitted active power *P* as well as receiving-end reactive power *Q* within the circle can be controlled by the UPFC, of course, with the rating limitation of series and shunt CMIs [28]. Several operating points of independent *P*/*Q* control

have been tested. Fig. 21(b) shows the phasor diagram for one of the test cases, case C1: $P = 0.25$, $Q = 0$, in this case, line current $\overrightarrow{I_L}$ is in phase with receiving-end voltage $\overrightarrow{V_R}$ due to zero receiving-end reactive power Q. In this case, the calculated line current amplitude is 7.5 A. Fig. 22 shows the corresponding experimental waveforms, (a) line current I_{La} and shunt CMI line voltage V_{Pab}, and (b) line current I_{La} and series CMI phase voltage V_{Ca}.

VI. Conclusion

This paper present a modulation and control method for the transformerless UPFC, which has the following features: 1) FFM of the CMI for extremely low THD of output voltage, low switching loss and high efficiency; 2) All UPFC functions, such as voltage regulation, line impedance compensation, phase shifting or simultaneous control of voltage, impedance, and phase angle, thus achieving independent active and reactive power flow control over the transmission line; 3) Dc capacitor voltage balancing control for both series and shunt CMIs; 4) Fast dynamic response ($<$10 ms). The transformerless UPFC with proposed modulation and control can be installed anywhere in the grid to maximize/optimize energy transmission over the existing grids, reduce transmission congestion and enable high penetration of renewable energy sources.

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